

Remarks:

Reconsideration of the application is requested.

Claims 1 and 3-8 are now in the application. Claims 1 and 3-4 have been amended. Claim 2 has been cancelled.

In the section entitled "Specification" on page 2 of the above-identified Office action, the Examiner has stated that the text "This produces a "bird's beak" 5 or a thickened area of the gate oxide 2 in the region below the side wall 22 of the gate 3" on page 11 is contradicted by FIG 2, in which no such thickened area is visible, as well as by FIG 3, in which there is no such thickened area below the gate oxide 2, instead, in FIG 3 the bird's beak 5 is located below the gate 3 itself.

Applicants respectfully disagree. In FIG 1, a cross-section of a preliminary form of a MOS transistor 20 having a gate oxide 2, a gate 3, for example made of polysilicon, and an insulating gate cover 4 which are produced on a substrate surface 21 of a semiconductor substrate I (see page 10, line 21 to page 11, line 2 of the specification) are shown. The oxide layer, which forms the gate oxide below the gate 3 is also present on the substrate surface outside the regions covered by the gate 3 and has an essentially uniform thickness

in both the areas covered by the gate 3 or the uncovered areas (see FIG 1).

It is described in the specification that an oxidation process is performed and FIG 2 shows the preliminary form of a MOS transistor 20 after such an oxidation process has been performed (see page 11, lines 9-10 of the specification). It becomes quite clear from FIG 2 that the thickness of the oxide layer 2 outside the areas covered by the gate 3 increases as a result of the oxidation process. This thickening of the oxide layer 2 also extends laterally into the area of the oxide layer covered by the gate 3 starting from the side walls 22. This produces the thickened areas or the bird's beak 5 shown in FIG 2. It is clear from FIG 2 that the thickness of the layer 2 is increased in the areas 5 immediately adjacent the side walls 22 when compared to the initial thickness of the gate oxide layer 2, which is preserved in the middle of the gate oxide 2 covered by the gate 3. Consequently, if one follows the line defined by side wall 22 of the gate 3 from the top in direction of the gate oxide 2, one reaches the point where the side wall 22 meets the top of the gate oxide covered by the gate 3. Clearly, this intersection is situated in the area of the side wall 22.

Furthermore, it is quite clear from FIG 2 that the thickness of the gate oxide 2 immediately below the side wall 22, i.e.

the area defined by the side wall if one extends the line defined by the side wall perpendicularly into the gate oxide 2, has a greater thickness than the gate oxide 2 below the middle section of the gate 3. The same argument clearly applies to FIG 3 in which the oxide layer 2 has been removed from the areas not covered by the gate 3.

Applicants are therefore of the opinion that there is no contradiction between the description on page 11 and FIGs 2 or 3.

In item 2 on pages 3-4 of the above-mentioned Office action, claims 1 and 5-6 have been rejected as being anticipated by Sun et al. (US Pat. No. 5,612,249) under 35 U.S.C. § 102(b).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. More specifically, the feature of claim 2 has been added to claim 1. The feature "having at least one side wall adjacent at least one of said conductive regions" can be clearly seen from FIGs 2-4 in which the side walls 22 are positioned adjacent the source/drain regions formed by the doped areas 6 and/or 8.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region and having at least one side wall adjacent at least one of said conductive regions; and

an insulating silicon nitride spacer disposed on said side wall of said gate, said spacer acting as an oxidation barrier;

said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below said side wall of said gate.

In amended claim 1, it has been clarified that the side wall (22) is positioned adjacent one of the conductive regions. Consequently, the thickened area (5) in the region below said side wall (22) is also positioned adjacent conductive region 6 and/or 8. Furthermore, it has been clarified that the insulating spacer is made of silicon nitride.

The fact that the thickened area is positioned adjacent the conductive regions is important to achieve the desired reduction of the leakage current, the so called GIDL (Gate Induced Drain Leakage). The thickening of the gate oxide 2 in the regions 5 results in a better insulation between the gate and the conductive region thereby reducing the leakage current. A reduced degree of leakage current between the conductive region and the gate results in a prolonged information retention time in single-transistor memory cells (see page 3, lines 1-7 of the specification).

Furthermore, the insulating spacer (7) is formed of silicon nitride. This enables the structuring of a self-aligned contact, for instance in a DRAM array, which allows the required minimal distance between two gates in such an array to be further reduced. With reference to the transistors shown in FIGs 3 and 4 of the instant application, it is clear that after the transistors shown therein have been formed they still need to be contacted, for instance by a bit line. This is usually achieved by depositing an insulating layer made of silicon oxide onto the transistors shown in FIGs 3 or 4 and subsequently etching vias into said silicon oxide insulating layer.

If the side wall spacer in the transistor is made of silicon oxide, great care must be taken to ensure that the openings in the etching mask used to form the vias are spaced at a sufficient distance from the side wall spacers. Otherwise these spacers would also be etched away during the via etch, exposing the side walls of the gate. Lithographic masks can only be produced within a certain level of exactness and the minimal distance which has to be observed between the via and the side wall spacer is determined by this degree of exactness. Consequently, this distance must include a safety margin taking into account the possible deviation of the

position of the via due to the use of the photolithographic etching mask.

This problem is avoided by the use of a silicon nitride spacer to protect the side walls of the gate stack. The etching of vias in the silicon oxide insulating layer is selective for silicon oxide. The silicon nitride spacer is not etched by this process. Consequently, there is no need for the safety margin and the distance between the gate and the via and the distance to the next gate in the array can therefore be further reduced.

Therefore, the MOS transistor now claimed in claim 1 combines a reduced leakage current with a reduced space requirement and therefore a higher possible level of integration on a substrate.

In contrast, in Sun et al. the transistors do not have a bird's beak in the region below the side wall adjacent the conductive regions of the transistor. This becomes apparent from Figures 18, 19, and 20 in combination with column 8, lines 19 to 28, in which it is explained that the left hand side of these figures show a cross-section in x-direction of the gate stack and the right hand side of these figures a cross-section in y-direction of the gate stack.

The cross-section in x-direction shows the position of the conductive regions 22 and/or 24 (N-LDD, P-LDD implants and n^+ , p^+ junctions of the transistor, see column 8, lines 29 to 53) in relation to the side walls and the field oxide bird's beak encroachment. It becomes clear from Figures 18 to 20 that the field oxide bird's beak encroachment is spaced away from the side walls of the gate stack which are positioned adjacent the conductive regions 22 and/or 24. To achieve this offset of the field oxide bird's beak encroachment under the active area, a nitride spacer 13 is used (see Figure 13 and column 6, lines 60 to 63). Therefore, Sun et al. do not disclose a transistor in which the gate oxide has a thickened area in a region below a side wall which is positioned adjacent a conductive region. Sun et al. disclose only transistors in which the gate oxide has thickened areas in regions below the side walls of the gate stack which are not adjacent the conductive regions of the transistor.

Furthermore, although the reference Sun et al. mentions the use of nitride spacers for achieving the offset of the field oxide bird's beak encroachment, it does not disclose the use of nitride spacers in the finished transistor. It is explicitly mentioned in Sun et al. that the spacers 23 shown in Figures 19 and 20 are made of an oxide material (see column 8, lines 40 to 42). Consequently, with the transistors

described by Sun et al. the formation of a self-aligned contact as described above is not possible.

Clearly, Sun et al. do not show "a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region and having at least one side wall adjacent at least one of said conductive regions; and an insulating silicon nitride spacer disposed on said side wall of said gate, said spacer acting as an oxidation barrier; said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below said side wall of said gate", as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over Sun et al. and since claims 5-6 are dependent on claim 1, they are believed to be patentable as well.

In item 4 on pages 4-5 of the above-mentioned Office action, claims 2-4 have been rejected as being unpatentable over Sun et al. in view of Ahmad (US Pat. No. 6,037,639) under 35 U.S.C. § 103(a).

Contrary to the Examiner's opinion, Ahmad does not disclose the use of silicon nitride spacers. Ahmad teaches the use of a second spacer 136, which is made of silicon oxide (see

column 5, lines 13 to 21 and Figs. 3 and 4). The vertical insulating spacer 126 is grown under conditions including a thermal oxidation, such that the spacer may contain oxide (see column 4, lines 33 to 34). Irrespective of the exact nature of the material of the so-called "spacer" 126, this protective vertical layer does not have a sufficient thickness to qualify as a spacer in the usual sense.

Consequently, although Ahmad uses the term "spacer" to describe this protective layer 126, it surely does not qualify as a spacer in the correct sense of the term and does not allow the formation of a self-aligned contact as described above in connection with the silicon nitride spacer of the instant application. As mentioned above, the proper side wall spacer of the transistor having a sufficient thickness to act as a spacer disclosed by Ahmad is the second spacer 136, which is made of silicon oxide.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 3-4 are dependent on claim 1, they are believed to be patentable as well. Claim 2 has been cancelled.

In item 5 on pages 5-6 of the above-mentioned Office action, claims 7-8 have been rejected as being unpatentable over Sun et al. in view of Krautschneider (US Pat. No. 5,854,500) under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 7-8 are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1 and 3-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

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Respectfully submitted


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Marked-Up Version of the Amended Claims:

Claim 1(amended). A MOS transistor in a single-transistor memory cell, comprising:

a semiconductor substrate having a substrate surface, a first conductive region and a second conductive region;

a gate oxide disposed on said substrate surface;

a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region and having at least one side wall adjacent at least one of said conductive regions; and

an insulating silicon nitride spacer disposed on said side wall of said gate, said spacer acting as an oxidation barrier;

said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below said side wall of said gate.

Claim 3(amended). The MOS transistor according to claim [2] 1, wherein said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer.

Claim 4 (amended). The MOS transistor according to claim [2]
1, wherein said gate includes a tungsten silicide layer and a
polysilicon layer.